



Semiconductor Technology: 3-Day Course Overview

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1. SEMICONDUCTOR JUNCTIONS:

Brief history of Semiconductors, 1940's - 1990's
Conductors; Semiconductors; Silicon Lattice structure.
Crystalline/Polycrystalline silicon; Valence diagrams.
Donors and Acceptors; Majority and Minority carriers.
Doping levels; Conductivity; Sheet resistance;
The P-N Junction: Contact potential & junction capacitance.
Abrupt & graded junctions; .
Junction breakdown: avalanche; punchthrough.
Gated-Junction Breakdown. LDD junction.
P+/N+ Junction - Zener Diode

2. MOS & BIPOLAR DEVICE STRUCTURES:

Bipolar Transistors: NPN formation, Junction depth; PNP.
Junction physical influences on Beta, Ft, Va, etc.
Gummel-Poon plot.
PNPN (SCR) structure; Latchup.
MOS Device structure & Formation;
MOS Oxides and Fixed Charges; CV Plot; Flatband Voltage
Threshold Voltage determination; Threshold Adjust implant;
Gamma or Body effect on Vt;
Gate oxide thickness; Oxide Breakdown;
Fowler-Nordheim Tunnelling; Hot electrons

3. CMOS PROCESS INTEGRATION :

A simple 5-mask metal-gate PMOS process
A 6-mask NMOS poly-gate process (self-aligned S/D)
A 7-mask basic CMOS process
Junction Isolation; Oxide Isolation (LOCOS).
LAMBDA design rules

4. OXIDATION:

Oxide types: Thermal (Dry v Wet), Deposited
Process sequence & equipment
Silicon Dioxide Lattice structure
Grove-Deal model of Oxidation; Linear/Parabolic growth
Growth-rate effects: Surface crystalline orientation
Addition of Chlorine
Limitations of Grove-Deal model; The Reisman model

5. DIFFUSION and ION IMPLANTATION:

Diffusion Kinetics; Activation Energies;
Vacancy/Interstitial Diffusion
Fick's First and Second Laws of diffusion;
Junction Depth; Lateral diffusion; erf/gaussian profiles
Diffusion Equipment; Ion Implantation Equipment
Advantages & Disadvantages of Ion Implantation;
Implant Physics; Channelling;
Substrate Damage; Annealing;
Transient-Enhanced Diffusion effect on Implant profiles

6. MASKING, PHOTORESISTS, PHOTOLITHOGRAPHY:

Pattern Generation: Optical vs E-Beam;
Positive/Negative Photoresists;
Resist processing: bake-expose-develop-etch-strip;
1X Mask types: Contact, Proximity, or Projection;
5X Reticles : Wafer 'stepper'
Optical Proximity correction
Depth-of-Focus & Resolution equations;
Optical/UV/Deep-UV/X-ray lithography

7. THIN FILM LAYER DEPOSITION:

Metallic Thin-Films: Al, Cu, W, Mo, Ta, Ti)
Dielectric Thin-Films: SiO₂, BPSG, TEOS, Si₃N₄
Film Requirements:
Deposition Methods: CVD, PVD, spin-on, Epitaxy
Growth-rate vs Temp; Diffusion vs Reaction rate
Low Pressure & Plasma Enhanced CVD
Epitaxial Silicon Growth/Deposition

8. METALLISATION and ETCHING:

Aluminium Deposition: PVD – Evaporation vs Sputtering
Al Step coverage, planarisation, tungsten plugs
Al stress-migration; Al Spiking;
Electromigration; Arrhenius Eqn; Current Density v Temp
Al-Si and Al-Cu alloys & phase diagrams
Interconnect Resistance & Capacitance; lateral scaling;
Etching Techniques: Wet-etch, Dry (plasma) etching;
Anisotropic Etching; Aspect Ratio; CD & Mask Bias
Nitric & Phosphoric Acid wet etching; crystal oriented etch;
Plasma Etch; Reactive Ion Etching (RIE)
Interconnect resistance and capacitance; Fringing;
Copper metalization; Single/Dual Damascene process
Chemical Mechanical Polishing (CMP); slurry grinding

9. VLSI PROCESS INTEGRATION & Modelling :

A sub-micron CMOS process flow
BiCMOS - Adding NPN to CMOS
Embedded memory integration issues:
SRAM, DRAM, EEPROM
Capacitors: Metal-Poly; Poly-Poly; Metal-Metal.
Linearity & Matching.
Varactors & Inductors; Q-Factor vs Metal thickness
Understanding a Wafer-Acceptance-Test (WAT) printout.
Defect Density, yield prediction and modelling
Process Modelling & Simulation: SUPREM; ATHENA

10. DEEP SUB-MICRON (DSM) PROCESSING:

0.25u -> 0.13u & beyond:

Lower Vdd and Vt voltages; Sub-Threshold leakage
Dual Gate oxides; Thin Gate oxide 'leakage' (tunnelling)
High-K gate materials;
Retrograde Wells; Triple Wells;
Analog Migration Issues: Gm*Ro degradation;
Salicide/Resistor value changes;
Pocket Implants; Dual-Pocket (Halo) vs Single-Pocket implants;
STI - Shallow Trench Isolation
Low-K dielectrics.
SOI – Silicon-on-Insulator; Bonded Wafers
Strained Silicon & Silicon-Germanium