



# Memory Design – Half-Day Tutorial

**DEMO:** ARTISAN Generator, and Mentor Graphics  
“Memory Builder” For RAM & ROM  
Limitations of Memory Compilers

**SRAM:** 6T Cell; “1T Cell”;  
Manhattan Layout  
Folded Bit Lines & Multiplex ratio  
Array/Periphery Ratio  
Read/Write Circuits  
Bit-Line Precharge, over-write prevention  
Sense Amp Design: - Linear  
- Latched  
- Cascoded Bit Lines

Synchronous Sram  
Dual-Port SRAM; same-cell contention  
SRAM Processes:  
- 4T w un-doped Poly pullups  
- 6T w Thin-Film (3D) P-ch;  
- Butting Contacts; Salicide:

**DRAM:** 1T/1C Cell  
Planar, Trench, Stacked Capacitors;  
CMOS with embedded DRAM  
EDO-DRAM; SDRAM; RDRAM;

**ROM:** 1T Cell  
Contact Programming  
Pseudo-Differential (Dummy bit-line)  
DDS ROMS; Rom Reduction Techniques

**EEPROM:** Non-Volatile Basics  
EPROM, EEPROM, Flash-EEPROM;  
Retention  
Endurance (max no R/W cycles)  
Case Study: EEPROM layout  
Erase – Byte/page/block?  
Charge Pumps, programming

**BIST:** Importance of Built-In-Self Test  
Examples: Address generation,  
Data comparators  
LFSR/signature speed testing  
Marching patterns,  
IddQ testing

New Memory Technology  
MRAM  
FRAM