



Mixed-Signal IC Design for Digital & ASIC Engineers

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	Day 1	Day 2	Day 3	Day 4	Day 5
9.00	page	2.1 p CMOS Modelling Threshold Voltage Device Equations Large Signal Models	3.1 p Amplifiers: 1 & 2 tr amplifiers; Frequency Response; CMOS vs BiCMOS	4.1 p Passives: R, L, C Matching: Centroiding, .	5.1 p CMOS Logic Types; Fanout; Metastability Tj; Pwr Diss; Θ_{ja} ESD Maps
10.30					
Break					
11.00	1.1 p <i>(Mon start 12.00)</i> Semiconductor Basics PN Junctions; NPN & MOS Devices	2.2 p Small-Signal Models; 2nd Order Effects SPICE models & accuracy	3.2 p Cascodeing; Diff Amps; OTA; PSRR/CMRR	4.2 p Filters: gmC, mosC Filters: Switched Capacitor Circuits	5.2 p Yield; Reliability; Deep Sub-Micron Manufacturability Halo/STI effects
12.30					
Break	<i>(Mon lunch 1.30-2.30)</i>				<i>Friday finish 12.30</i>
1.30	1.3 LAB p SIMPLer Mask Layout & Process Design-NPN & dual Gate Ox NMOS	2.3 LAB p Schematic Entry; MOS I-V SPICE Simulation	3.3 LAB p SPICE Inverter Amp; OP-Amp Design, Gain, BW sims	4.3 LAB p Inverter Layout; LVS; DRC; Matching; Diff Amp Layout;	
3.00					
Break					
3.30	1.4 p Oxidation, Diffusion, Ion Implant; Photolithography, Metal, Dielectrics	2.4 p CMOS Subcircuits: Switches; lev-shift; Current Sources I & V References	3.4 p 2-Stage Amplifier Low-Voltage deep sub micron analog design	4.4 p Noise & Crosstalk in mixed-signal systems	Biggest circuit in course is 5 transistors ...
5.00					