



# Course Overview & Table of Contents

	Day 1	Day 2	Day 3	Day 4	Day5
9.15	<b>1.1</b> page 7 <b>Semiconductor Basics</b> PN junctions NPN Bipolar formation	<b>2.1</b> p 79 <b>CMOS Modelling</b> Threshold Voltage Device Equations Large Signal Models	<b>3.1</b> p 133 <b>Amplifiers:</b> 1 & 2 tr amplifiers; Frequency Response; CMOS vs BiCMOS	<b>4.1</b> p 189 <b>Passives:</b> R, L, C Matching: Centroiding, .	<b>5.1</b> p 267 <b>CMOS Logic Types;</b> Fanout; Metastability Tj; Pwr Diss; $\theta_{ja}$ ESD Maps
10.45					
Break					
11.15	<b>1.2</b> p 25 MOS Devices CMOS processes Oxidation Diffusion/Implantation	<b>2.2</b> p 92 Small-Signal Models; 2nd Order Effects SPICE models & accuracy	<b>3.2</b> p 147 Cascodeing; Diff Amps; OTA; PSRR/CMRR	<b>4.2</b> p 208 <b>Filters:</b> gmC, mosC Filters: Switched Capacitor Circuits	<b>5.2</b> p 290 <b>Yield; Reliability;</b> Deep Sub-Micron Manufacturability Halo/STI effects
12.45					
Break					
2.00	<b>1.3 LAB</b> p 47 SIMPLer Mask Layout &Process Design-NPN &dual Gate Ox NMOS	<b>2.3 LAB</b> p 106 Schematic Entry; MOS I-V SPICE Simulation	<b>3.3 LAB</b> p 161 SPICE Inverter Amplifier simulations: Gain, BW, delay sims	<b>4.3 LAB</b> p 227 Inverter Layout; LVS;DRC	<b>5.3 LAB</b> p 315 Diff Amp Layout; Matching, Interdigitating
3.30					
Break					
4.00	<b>1.4</b> p 58 Photolithography; Back-End processing: Metal, Dielectrics, Etching	<b>2.4</b> p 115 <b>CMOS Subcircuits:</b> Switches; lev-shift; Current Sources I & V References	<b>3.4</b> p 173 2-Stage Amplifier Low-Voltage deep sub micron analog design	<b>4.4</b> p 245 <b>Noise &amp; Crosstalk</b> in mixed-signal systems	<b>5.4 LAB cont'd</b> p OP-Amp design cont;d - Gain, Offset, freq response, 1
5.30					